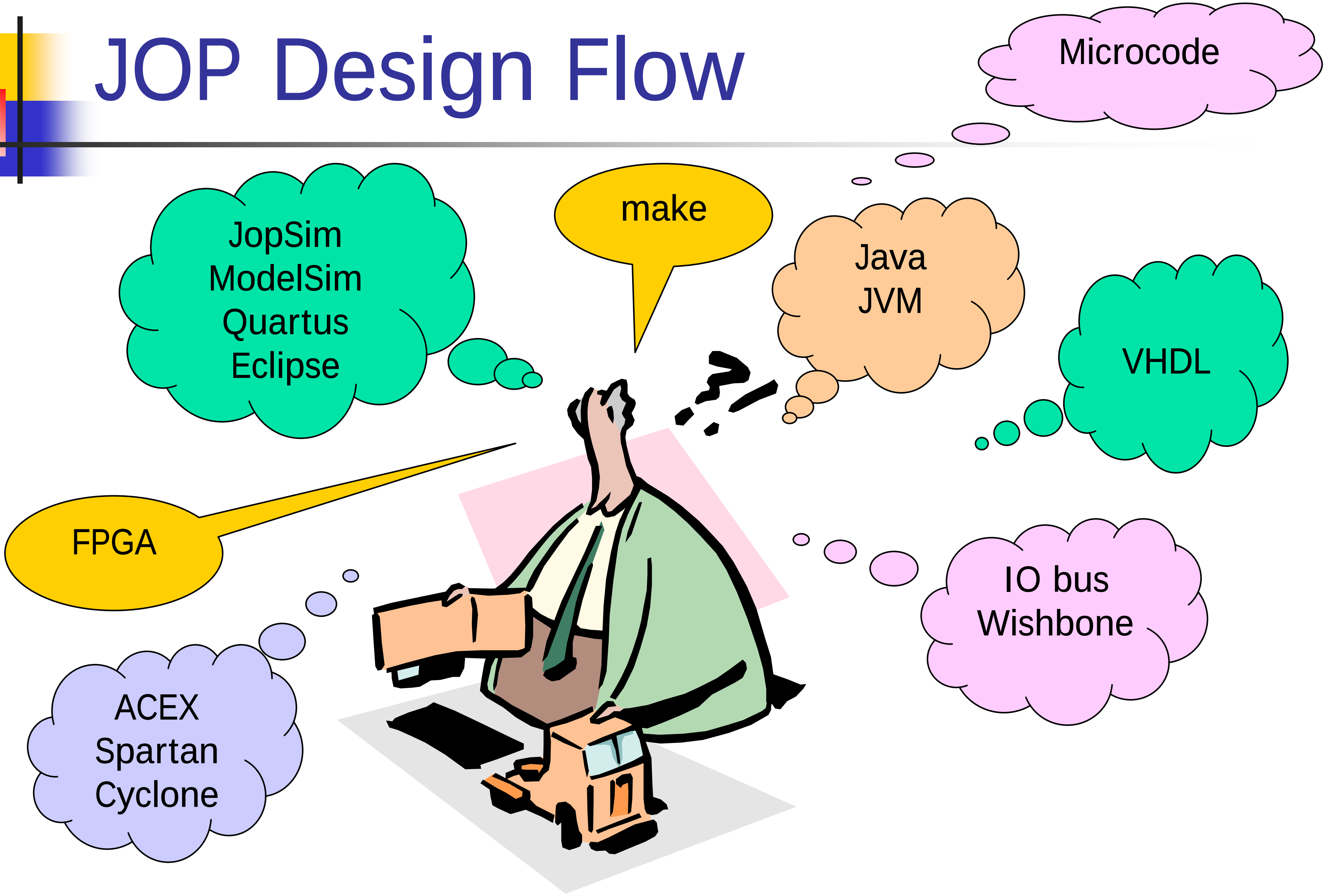
JOP Design Flow



Microcode

JopSim
ModelSim
Quartus
Eclipse

make

Java
JVM

VHDL

FPGA

IO bus
Wishbone

ACEX
Spartan
Cyclone

The Project

- 4/5 programming languages
  - VHDL, Java, Microcode, C, (Verilog)
- 267 directories, 1403 files
- 68k LOC
  - find . –name *.vhd – print | xargs wc
  - Java: 30565
  - VHDL: 23080
  - Microcode (.asm): 10089
  - C: 4141
- 4 FPGA types, 6 target boards

Don‘t Panic

- This complexity is not unusual
  - Linux kernel: 6M LOC!
- There is a master `Makefile`
  - A single target can be built
  - Calls batch files
- Help
  - *Some* documentation is available (pdf and web)
  - e-mail to Schoeberl
  - Yahoo! Groups : java-processor

Directories

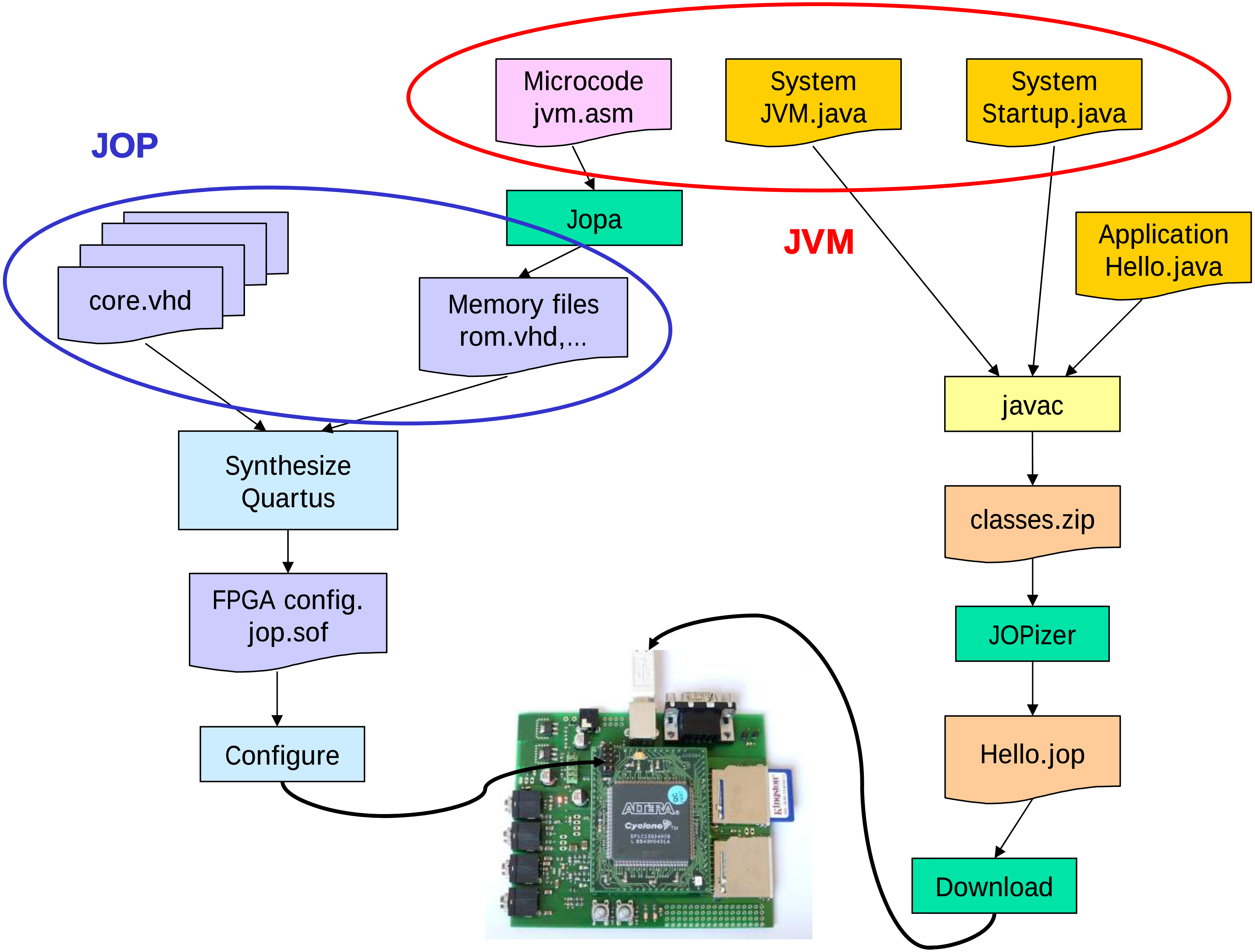
- vhdl
  - The hardware description of JOP
- asm
  - The JVM in microcode
- java
  - System sources (JVM, JDK)
  - Target applications
  - Tools

Directories cont.

- quartus
  - Project files for Altera FPGA boards
  - Each board and variation in its own directory
- xilinx
  - Project files for Xilinx FPGA boards

File Types

- Source
  - .asm, .vhd, .java
- Generated
  - JVM assembly: .vhd, .mif, .dat
  - Quartus: .sof, ...
  - JOPizer: .jop
- Configuration
  - Project: Makefile, .bat
  - Quartus: .qsf, .cdf



JOP

JVM

Microcode
jvm.asm

System
JVM.java

System
Startup.java

Jopa

Application
Hello.java

core.vhd

Memory files
rom.vhd,...

javac

Synthesize
Quartus

classes.zip

FPGA config.
jop.sof

JOPizer

Configure

Hello.jop

Download

JOP Startup

- FPGA configuration
  - ByteBlaster download cable
  - USB
  - Flash on power up
    - Watchdog -> PLD configures FPGA
- Java application
  - Serial line
  - USB
  - Flash

Startup Configuration

- FPGA configuration
  - PLD (MAX7064)
  - ByteBlaster: cyc_conf_init.pof
  - Flash: cyc_conf.pof
- Java application
  - JVM (jvm.asm) on startup
    - Loads the application (.jop)
    - Defines download type
    - Constants: FLASH, USB, SIMULATION

Targets

- Top level defines FPGA type
  - jopcyc.vhd
  - jopcyc12.vhd
  - jopacx.vhd
  - ...
- IO top level defines board type
  - scio_min.vhd
  - scio_baseio.vhd
  - scio_dspio.vhd
  - ...

JVM + Library

- JVM
  - Microcode (jvm.asm)
  - Java (JVM.java, Startup.java, GC.java)
- Library
  - JOP specific: util, ejip, joprt
  - JDK: System, String,...

Native Functions

- Bridge between Java and the HW
  - Memory, IO access
  - Register, stack cache
- Special bytecode
- Implemented in microcode
- Translated in JOPizer
- Define in:
  - jvm.asm
  - com.jopdesign.sys.Native.java
  - com.jopdesign.tools.JopInstr.java

Simulation

- VHDL with ModelSim
  - HW related changes
  - Testbench reads the memory content
- High level with JopSim
  - System debugging (e.g. GC)
  - Reads .jop files
  - A JVM in Java
- Board simulation

Summary

- Modules
  - JOP – VHDL files
  - JVM – Microcode + Java
  - Application – Java
- Build
  - Jopa, Quartus -> FPGA configuration file (.sof)
  - javac, JOPizer -> Java application file (.jop)
  - Makefile + Batchfiles

More Information

- An Introduction to the Design Flow for JOP